

FEATURES & BENEFITS

- Accurate capture of 8.0 GT/s, 5.0 GT/s, and 2.5 GT/s
- Decode all PCI Express traffic including TLP, DLLP and ordered sets
- LTSSM state and sub-state diagrams to help identify and troubleshoot link-up issues
- Interposers supported: slot/AIC, U.2 (SFF-8639), M.2, SFF-8644 (coming soon)
- Complete and precise protocol capture and analysis of PCIe (up to Gen3) and Non-Volatile Memory Express (NVMe)
- Dedicated appliance; no swapping blades or modules
- Portable: Micro easily fits in a briefcase

ADVANTAGES

- Zero Calibration. It just works.
- Traces is up and usable immediately. Download *later*.
- Breakthrough hardware can
 - Filter by BDF
 - Trigger on native NVMe
 - Immediately render NVMe without a boot trace
- Built-in eye diagram display
- Easily search for specific packets, primitives, ordered sets, addresses, or other events with the Quick Search and Advanced Search functions
- Field layouts matching the PCI Express specifications
- Buffer sizes up to 72 GB
- Lower TCO with standard cables and innovative interposers

SerialTek provides two market-leading PCI Express® (PCIe®) analysis solutions, the BusXpert PRO and the BusXpert Micro II (see figure 1), for PCIe (including Non-Volatile Memory Express® or NVMe) technology design and validation, including host bus storage adapters, computer systems, servers, and storage products. All SerialTek PCIe analysis products are compliant with the PCIe 1.x, 2.x and 3.0 specifications.

SerialTek analyzers “passively” capture all PCIe bus traffic without re-timing or re-transmitting bus signals—there is no masking or “cleaning up” of low-level link issues. In addition, SerialTek’s proprietary hardware natively captures, filters, triggers, and decodes BDFs and NVMe queues **without**

the need to capture boot-up. And development cycles are shortened because everything – including NVMe! – is ready to view in seconds (no need to save off the trace, first), and BusXpert’s intuitive software interface virtually eliminates the learning curve.


Several cost-effective and flexible PCIe interposers are available for BusXpert Analyzer users. High signal integrity on these industry-leading products means that users can capture PCIe and NVMe traffic via add-in card (AIC) (also known as “Slot” or “Card Edge”), U.2 (SFF-8639), and M.2 interposers at speeds of 8.0 GT/s (Gen3), 5.0 GT/s (Gen2), and 2.5 GT/s (Gen1) with **zero configuration**. This contrasts greatly with competing solutions with a nearly impossible number of interposer and signal equalization options. The REFCLK is also brought out to oscilloscope connectors for CEM-level development and troubleshooting.


Low-cost SFF-8644 cables are used to connect the interposers to the SerialTek PCIe Analyzer. Unlike competing cables, which are bulky and can cost thousands, SFF-8644 cables are reliable, cost-effective, and easy to handle – an important factor in any PCIe® analyzer total cost of ownership (TCO) calculation.



Figure 1: The BusXpert Micro 2 PCIe/NVMe Analyzer measures 7 inches x 10 inches x 2

Analyzer Specifications

x4 Micro II PCIe Analyzer		
	Model Numbers	PE-1MIA2-0403
	Trace Buffer (Maximum)	36GB
	Data Rates Supported	2.5, 5.0, and 8.0 GT/s
	Widths Supported	x1, x2, x4
	Front Panel LEDs	PCIe Status: Activity, TLP, ERR STS, CRC ERR Coding Err, Training; Speed: Gen1, Gen2, Gen3; Analyzer: Config, Ethernet, USB, Run, Trigger.
	Impedance (Differential)	95 Ohms (+/- 5%)
	Power	19.5V-9.23A; 180W Max Power (External Switching Power Adapter provided by SerialTek)
	Dimensions	7in (width) x 10in (depth) x 2in (height) / 178mm x 254mm x 51mm
	Weight	4.5 lbs / 2 kgs
	Environmental	Operating: 40 Degrees C Max Ambient Temperature

x8 PRO PCIe Analyzer		
	Model Numbers	PE-1PRA1-080318-000
	Trace Buffer (Maximum)	72GB
	Data Rates Supported	2.5, 5.0, and 8.0 GT/s
	Widths Supported	x1, x2, x4, x8
	Front Panel LEDs	PCIe Status: Activity, TLP, ERR STS, CRC ERR Coding Err, Training; Speed: Gen1, Gen2, Gen3; Analyzer: Config, Ethernet, USB, Run, Trigger.
	Impedance (Differential)	95 Ohms (+/- 5%)
	Power	100-240VAC 47-63Hz; 500W Max
	Dimensions	16 in(depth) x 14 in (width) x 3.5" (height) / 406mm x 356mm x 89mm
	Weight	14.5 lbs / 6.6 kgs
	Environmental	Operating: 40 Degrees C Max Ambient Temperature

Interposers

x4, x8 AIC (Slot, Card Edge)	x4 U.2 (incl. dualport)	x4 M.2
		



FEATURES & BENEFITS

- Interposers offered include: AIC (slot), M.2, and U.2. SFF-8644 coming soon
- Compliant with PCI Express 1.x, 2.x and 3.0 specifications
- Designed to capture PCIe® and NVMe® data at 8.0 GT/s, 5.0 GT/s and 2.5 GT/s
- Zero calibration required
- “Passive” tapping to avoid masking, hiding, or “cleaning up” electrical and/or link issues

ADVANTAGES

- Adaptive slot interposers operate at various bus widths providing significant overall solution cost savings; a SerialTek x8 slot interposer can operate at x1, x2, x4, and x8 with *or without* card reducer edge adapters. The x4 can operate at x1, x2, and x4
- A single U.2 (SFF8639) interposer provides both dual-port (2x2) and single-port (x1, x2, or x4) analysis
- U.2 interposer comes in standard and extended lengths to accommodate all drive bays
- Low-cost, flexible, high performance cabling for reliable analyzer-to-interposer connections provides real cost advantages over competing solutions that use cumbersome, bulky, and expensive iPass-type cabling
- Mini-SMP outputs for REFCLK# (varies by model)

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Several cost-effective and flexible PCIe® Interposer options are available. These interposer solutions are designed to provide maximum performance with minimal configuration

when capturing PCI Express communication data between hosts and devices. SerialTek’s latest generation of x4 interposers delivers top performance with zero user-side calibration required.

The most commonly used interposer is the add-in card (AIC) form-factor (also known as “Slot” or “Card Edge”). High signal integrity on this industry-leading interposer makes it ideal not only for AIC PCIe analysis but also for M.2, U.2 (SFF-8639), and other PCIe connectors via adapters.

In addition to AIC, SerialTek provides native U.2 and M.2 interposers. The U.2 interposer combines single-port (1x4) and dual-port (2x2) functionality and is compatible with SSD carriages, creating a perfect fit in any server. The U.2 interposer also comes in two depths to accommodate all drive bay geometries. The M.2 interposer has four Host/Socket adapters (HSAs) for all current M.2 form factors.

All BusXpert interposers provide header pins to select sideband signals for analysis and a REFCLK-oscilloscope SFL interface. Low-cost SFF-8644-based cabling connects the interposer to the Analyzer. All interposers are compatible with both the BusXpert PCIe/NVMe PRO (part number PE-1PRA1-080318-000) and BusXpert PCIe/NVMe Micro II (part number PE-1MIA2-0403) Analyzers.

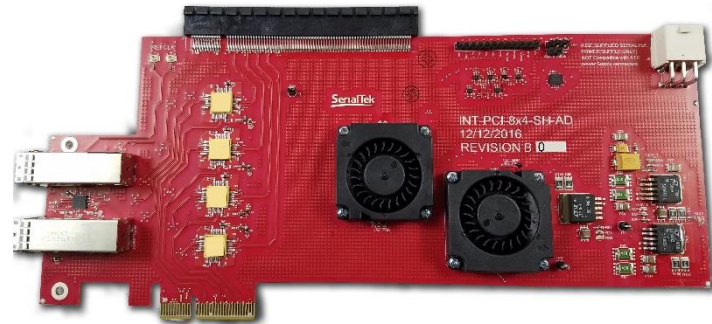


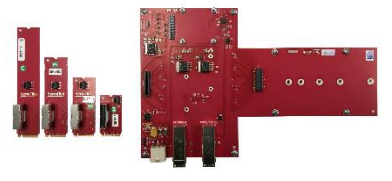


Figure 1: PCIe Gen3 x4, x8 Slot/AIC Interposer.

Interposer and Analyzer Specifications

x4, x8 AIC/Slot Interposer		
	Model Numbers	PE-1SLI1-0304-000, PE-1SLI1-0308-000
	Specification Compliancy	PCIe 1.x, 2.x, 3.0
	Data Rates Supported	2.5, 5.0, and 8.0 GT/s
	Widths Supported	x1, x2, x4
	Analyzer Connector	SFF8644 (SerialTek proprietary)
	Impedance (Differential)	95 Ohms (+/- 5%)
	Power	12V DC External
	Dimensions	9.9 in (length) x 3.6 in (height) / 251mm x 91mm
	Weight	5.4 oz / 153 grams
x4 U.2/SFF8639 Interposer		
	Model Numbers	PE-2U211-0304-000
	Specification Compliancy	PCIe 1.x, 2.x, 3.0
	Data Rates Supported	2.5, 5.0, and 8.0 GT/s
	Widths Supported	x1, x2, x4
	Analyzer Connector	SFF8644 (SerialTek proprietary)
	Impedance (Differential)	95 Ohms (+/- 5%)
	Power	12V DC External
	Dimensions (Length x Width (nose length))	Standard: 13.25in x 6.50in (5.375in) 337mm x 165mm (136mm) Extended: 17.50in x 6.50in (9.376in) 445mm x 165mm (238mm)
Weight	13.10 oz / 371 grams	
x4 M.2 Interposer		
	Model Numbers	PE-1M211-0304-000
	Specification Compliancy	PCIe 1.x, 2.x, 3.0
	Data Rates Supported	2.5, 5.0, and 8.0 GT/s
	Widths Supported	x1, x2, x4
	Analyzer Connector	SFF8644 (SerialTek proprietary)
	Impedance (Differential)	95 Ohms (+/- 5%)
	Power	12V DC External
	Dimensions	9.9 in (length) x 3.6 in (height) / 251mm x 91mm
Weight	5.4 oz / 153 grams	



FEATURES & BENEFITS

- Fast: traces come up in seconds – even NVMe
- Optimized: see PCIe and NVMe configuration and transactions without capturing bootup (incl. hotswap)
- Configurable: drag, drop, dock, and resize views. Customize colors to highlight key events. Hide or rearrange columns
- Clean: debug faster using only the views you choose
- Free: software support is free and always will be. Colleagues download the full software at no additional cost

SerialTek provides two market-leading PCI Express® (PCIe®) analysis solutions, the BusXpert PRO and the BusXpert Micro II, for PCIe (including Non-Volatile Memory Express® or NVMe) technology design and validation, including host bus storage adapters, computer systems, servers, and storage products. All SerialTek PCIe analysis products are compliant with the PCIe 1.x, 2.x and 3.0 specifications.

For all of the PCIe BusXpert’s hardware innovations, it’s in working with the captured trace that the BusXpert truly shines. Multiple views at various layers of abstraction give a customizable display of the trace. One-click Quick Show, Hide, and Search; Advanced Search, Show, and Hide; one-click toggling between PCIe, NVMe, LTSSM, Upstream, and Downstream—and much more—all work to expedite trace analysis.

Figure 1 (right): Transaction View aggregates all events in a transaction and expands to show individual events. Configurable columns give additional information.

Time	Channel	Command	Status	Transfer Size	Data Preview	Speed
13.802.420.053.000	[Down 1, Up 1]	Memory Read Request	Successful Completion	4 0000000h		8.0
13.803.430.555.000	[Down 1, Up 1]	Memory Read Request	Successful Completion	4 0000000h		8.0
13.804.441.963.000	[Down 1, Up 1]	Memory Read Request	Successful Completion	4 0000000h		8.0
13.804.442.047.000	Down 1	TLP Memory Read Request (0x822)				
13.804.614.400.000	Up 1	DLLP Ack (0x822)				
13.804.614.442.000	Down 1	TLP Completion With Data (0x819)				
13.804.615.078.000	[Down 1, Up 1]	Memory Write Request	Transaction Complete	4 0000000h		8.0
13.804.615.078.000	Down 1	TLP Memory Write Request (0x823)				
13.804.615.164.500	Up 1	DLLP Ack (0x823)				
13.804.615.129.000	[Down 1, Up 1]	Memory Read Request	Successful Completion	4 0000000h		8.0
13.804.615.654.000	[Up 1, Down 1]	Memory Read Request	Successful Completion	64 00000009h 00000000h 0...		8.0
13.804.653.788.500	[Up 1, Down 1]	Memory Write Request	Transaction Complete	16 007f007fh 00000000h 00...		8.0
13.804.654.826.500	[Up 1, Down 1]	Message Request Local - Terminate at Receiver	Transaction Complete	0		8.0
13.805.626.487.500	[Down 1, Up 1]	Memory Write Request	Transaction Complete	4 0000000h		8.0
13.805.628.392.500	[Up 1, Down 1]	Message Request Local - Terminate at Receiver	Transaction Complete	0		8.0
13.805.628.392.500	Up 1	TLP Message Request Local - Terminate at Receiver (0x81e)				
13.805.628.434.500	Down 1	DLLP Ack (0x81e)				
13.805.629.259.500	[Down 1, Up 1]	Memory Write Request	Transaction Complete	4 00000002h		8.0

Bit	Field	Value
7	Fmt	0 (3 DW header, no data)
6	Type	00 (MRd)
5	Reserved	0
4	TC	0 (Best Effort)
3	Reserved	0
2	Attr[2]	0 (Default)
1	LN	0
0	TH	0 (Default)
2	TD	0 (Default)
1	EP	0 (Default)
0	Attr[1]	0 (Default)
0	Attr[0]	0 (Default)
0	AT	0 (Default/Untranslated)
0	Length	001
0	Requester ID	0000
0	Tag	00
0	Last DW BE	0
0	1st DW BE	F
0	Address	DFC3001C

Figure 2 (left): Details View displays the fields in an event as they appear in the specification. Display values in binary, decimal, or hex; change the bit width; define your own events complete with custom field names.

Figure 3 (right): Data View displays individual bits in an event as binary, decimal, or hex. Control the endianness, display bits as Bytes, Words, or DWORDs, and ASCII. See only the payload or the entire packet. Compare data from different transfers. Search for specific string of values within the packet.

Packet	Hex	Bin	Dec	BYTES	WORDS	DWORDs	Big Endian	Little Endian	Bytes per row	Search data
00000000	005F	2468	0000	0100	.._sh....				8	
00000008	0000	0F00	C3DF	1C00					
00000010	1899	FDD1							

Spreadsheet View

Time	Down	Up	Link...	Format	Type	Completion Status	Requester ID	Completer ID	Data Preview	Ad
13.800.408.025.000		TLP (0x815)	1	3 DW header, with data	CpID	0 (Successful Completion)	0x0	0x700	0x00000000	
13.800.408.067.000	DLLP (0x815)		1		Ack					
13.801.408.979.000	TLP (0x81f)		1	3 DW header, no data	MRd		0x0			
13.801.409.066.500		DLLP (0x81f)	1		Ack					
13.801.419.010.500		TLP (0x816)	1	3 DW header, with data	CpID	0 (Successful Completion)	0x0	0x700	0x00000000	
13.801.419.052.000	DLLP (0x816)		1		Ack					
13.802.420.053.000	TLP (0x820)		1	3 DW header, no data	MRd		0x0			
13.802.420.141.000		DLLP (0x820)	1		Ack					
13.802.429.883.000		TLP (0x817)	1	3 DW header, with data	CpID	0 (Successful Completion)	0x0	0x700	0x00000000	
13.802.429.925.000	DLLP (0x817)		1		Ack					
13.803.430.555.000	TLP (0x821)		1	3 DW header, no data	MRd		0x0			
13.803.430.642.500		DLLP (0x821)	1		Ack					
13.803.440.838.000	TLP (0x818)		1	3 DW header, with data	CpID	0 (Successful Completion)	0x0	0x700	0x00000000	
13.803.440.879.500	DLLP (0x818)		1		Ack					
13.804.441.963.000	TLP (0x822)		1	3 DW header, no data	MRd		0x0			
13.804.442.047.000		DLLP (0x822)	1		Ack					
13.804.614.400.000		TLP (0x819)	1	3 DW header, with data	CpID	0 (Successful Completion)	0x0	0x700	0x00000001	

Figure 4 (left): Spreadsheet View displays events from all lanes, one event per row, in chronological order.

Lane View

Time	Dn 1 Sym	Dn 1 Lane 0	Dn 1 Lane 1	Dn 1 Lane 2	Dn 1 Lane 3	Up 1 Sym	Up 1 Lane 0	Up 1 Lane 1	Up 1 Lane 2	Up 1 Lane 3
13.725.561.586.000	2	LCRC 60	LCRC 16	LCRC 52	LCRC A0					
13.725.561.587.000	3	TLP Length[3:0]:5,ST... SF	TLP Length[10:4]:00 00	Frame CRC:6,Seque... 67	Sequence Number[7:0] D4					
13.725.561.588.000	4	3 DW header, no data... 00	Best Effort,Default:LN... 00	Default:Default,Defau... 00	Length[7:0] 01					
13.725.561.589.000	5	Requester ID[15:8] 00	Requester ID[7:0] 00	Tag:00 00	Last DW BE:0,1st DW... 0F					
13.725.561.590.000	6	Address[31:24] DF	Address[23:16] C3	Address[15:8] 00	Address[7:0] 1C					
13.725.561.591.000	7	LCRC FC	LCRC F5	LCRC DB	LCRC B1					
13.725.561.668.000						11	SDP Token F0	SDP Token AC	Ack 00	Reserve 00
13.725.561.669.000						12	AckNak_Seq_Num[1... 07	AckNak_Seq_Num[7... D3	16-Bit CRC[15:8] 7E	16-Bit CRC F2
13.725.561.678.000						5	SDP Token F0	SDP Token AC	Ack 00	Reserve 00
13.725.561.679.000						6	AckNak_Seq_Num[1... 07	AckNak_Seq_Num[7... D4	16-Bit CRC[15:8] 19	16-Bit CRC 80
13.725.587.436.500						1	TLP Length[3:0]:6,ST... 6F	FP,TLP Length[10:4]:... 80	Frame CRC:2,Seque... 27	Sequence Num... CB

Figure 5 (right): Lane View displays data as it comes across the bus. Low-level striping of data can be easily examined and verified.

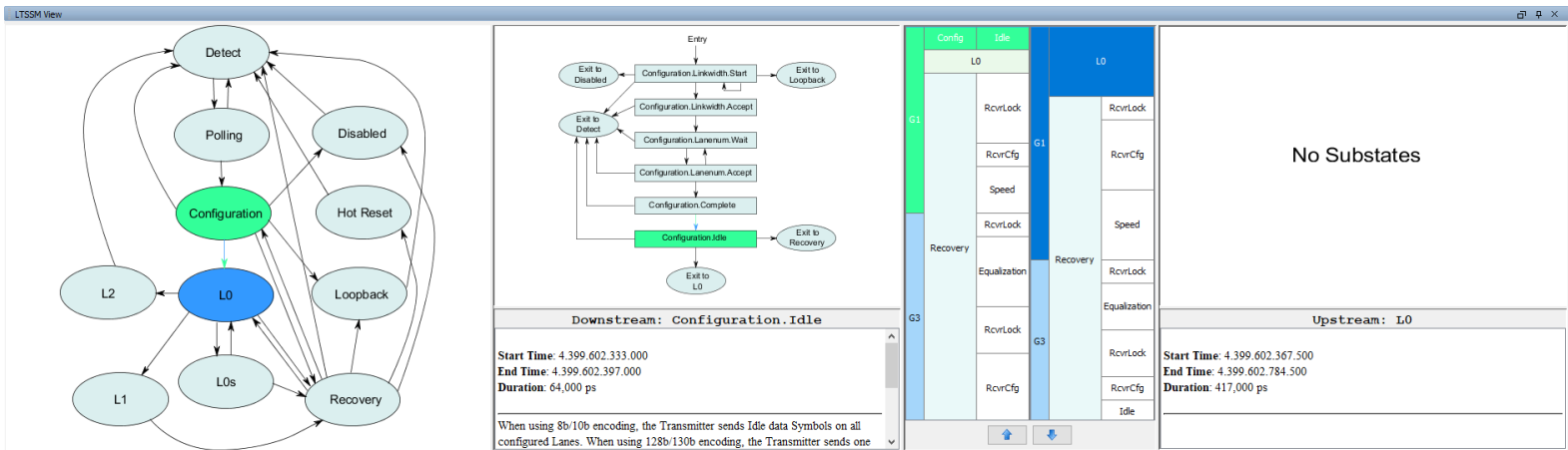


Figure 6 (above): LTSSM View displays Main- and Sub-state, entry and exit times, and descriptions of each state. Point and click to search LTSSM states and transitions and synchronize other views to a given state.



FEATURES & BENEFITS

- Fast: traces come up in seconds – even NVMe
- Optimized: see PCIe and NVMe configuration and transactions without capturing bootup (incl. hotswap)
- Intelligent: trigger and filter on actual NVMe events without false-positives
- Free: software support is free and always will be. Colleagues download the full software at no additional cost

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The SerialTek BusXpert PCIe/NVMe Analyzer is the first and only protocol analyzer designed from the ground up to analyze NVMe. It should come as no surprise, then, that BusXpert for NVMe is the best NVMe analyzer in the world, bar none. Only the BusXpert can

- Detect and decode NVMe *on the fly*, including hotswap
- Pre-capture filter selected Bus Device Functions (BDFs)
- Trigger on packets to/from specific BDF(s), incl. NVMe devices and queue(s)
- Display decoded NVMe (and PCIe) seconds after capture completes

AUTODETECT NVMe

Patent-pending technology exclusive to the BusXpert automatically identifies each Bus Device Function – including devices removed from or added to the bus – prior to, during, and after capture. This information is then used to determine the BDF source or destination for all PCIe bus traffic, *on the fly*. This gives BusXpert a level of precision unmatched by any other PCIe or NVMe protocol analyzer.

Figure 1. Without capturing boot-up, the following information is automatically captured by BusXpert: Config Space (below left), NVMe Queues (below center), Controller Registers (below right)

Config Space	Controller Registers	NVMe Queues
7	Vendor ID: 8086	
6	Device ID: 0953	
5	Reserved: 00	
4	Capabilities List: 1	
3	Interrupt: 0	
2	Revision ID: 01	
1	Class Code: 010802 (NVMe Express)	
0	Cache Line Size: 00	

Queue Type	Queue ID	Queue Size (# of Entries)	Base Address	Valid From	Valid To
I/O Completion	0x01	0xff	8cd23000	17.300.843.388.000	End of Recording
I/O Submission	0x01	0xff	8cd1e000	17.301.848.099.500	End of Recording
Admin Submission	0x00	0xff	8cd2b000	17.296.820.271.000	End of Recording
Admin Completion	0x00	0xff	8cd26000	17.296.820.271.000	End of Recording

Register	Value
0	Reserved: 00000000
1	Reserved: 00000000
2	Reserved: 00000000
3	Interrupt Vector Mask Set: 00000000
4	Interrupt Vector Mask Clear: 00000000
5	Reserved: 00000000
6	Memory Page Size: 0 (4KB)
7	I/O Command Set Selected: 0 (NVMe Command Set)
8	Reserved: 0
9	Enable: 1 (Enabled)
10	Shutdown Notification: 0 (No Notification; no effect)
11	Arbitration Mechanism Selected: 0 (Round Robin)
12	I/O Completion Queue Entry Size: 4
13	I/O Submission Queue Entry Size: 6
14	Reserved: 00
15	Reserved: 00000000
16	Processing Paused: 0 (Processing)
17	NVM Subsystem Reset Occurred: 0
18	Shutdown Status: 0 (Normal operation)
19	Controller Fatal Status: 0 (No Errors)
20	Ready: 1 (Ready)
21	Reserved: 00000000

FILTER BY BDFS

The ability to determine the BDF source or destination of every Transaction Layer Packet (TLP) on the bus allows BusXpert PCIe to pre-capture filter by BDF and/or NVMe queue – a capability unmatched in the industry. Users can select from auto-detected BDFs and queues, or manually enter their own.

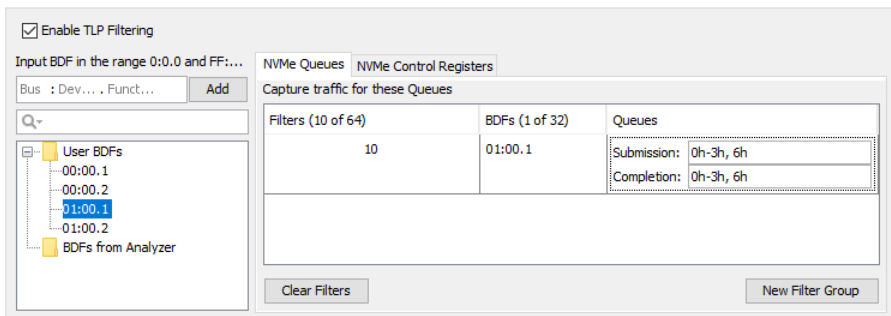


Figure 2. TLP Filtering allows users to select which BDFs and/or NVMe queues are included in the trace. This interface is also used to refine TLP trigger events to specific BDFs and queues, eliminating false-positive triggers commonly associated with NVMe triggering.

TRIGGER ON PACKETS TO/FROM SELECTED BDFS AND NVMe QUEUES

The same interface used in the pre-capture filter (figure 2, above) is also used in the creation of triggers based on NVMe queues and PCIe BDFs. By specifying a BDF and queue, random TLP payload data no longer results in a false trigger. No other PCIe analyzer can do this.

INSTANT NVMe. NO NEED TO WAIT.

SerialTek’s breakthrough BusXpert hardware allows the decode and display of NVMe within seconds of trace capture. There is no need to wait hours for a trace to save and post-process – only to discover that a new trace is needed.

Figure 3. NVMe Transactions are decoded and displayed in moments in BusXpert Transaction View. Expand transactions in one click to display the underlying PCIe side-by-side with the corresponding NVMe.

Time	Channel	Command	Status	Transfer Size	Data Preview	Speed	Tag	Address/Reg	Rd
17.296.812.551.500	[Down 1, Up 1]	NVMe: Read Controller Capabilities	Successful Completion	4 28010ffffh	8.0	0000h	DF010000h	00	
17.296.813.135.500	[Down 1, Up 1]	NVMe: Read Controller Configuration	Not Enabled	4 00000000h	8.0	0000h	DF010014h	00	
17.296.813.717.500	[Down 1]	NVMe: Write Controller Configuration	Not Enabled	4 00460000h	8.0	0000h	DF010014h	00	
17.296.819.423.000	[Down 1]	NVMe: Write Admin Queue Attributes	Transaction Complete	4 00ff00ffh	8.0	0000h	DF010024h	00	
17.296.819.492.000	[Down 1]	NVMe: Write Admin Submission Queue Base Address	Transaction Complete	4 8cd2b000h	8.0	0000h	DF010028h	00	
17.296.819.545.500	[Down 1]	NVMe: Write Admin Submission Queue Base Address	Transaction Complete	4 00000000h	8.0	0000h	DF01003Ch	00	
17.296.819.594.500	[Down 1]	NVMe: Write Admin Completion Queue Base Address	Transaction Complete	4 8cd26000h	8.0	0000h	DF010030h	00	
17.296.819.668.000	[Down 1]	NVMe: Write Admin Completion Queue Base Address	Transaction Complete	4 00000000h	8.0	0000h	DF010034h	00	
17.296.819.716.500	[Down 1, Up 1]	NVMe: Read Controller Configuration	Not Enabled	4 00460000h	8.0	0000h	DF010014h	00	
17.296.820.314.000	[Down 1]	NVMe: Write Controller Configuration	Enabled	4 00460000h	8.0	0000h	DF010014h	00	
17.296.820.363.000	[Down 1, Up 1]	NVMe: Read Controller Status	Not Ready	4 00000000h	8.0	0000h	DF01001Ch	00	
17.297.821.792.500	[Down 1, Up 1]	NVMe: Read Controller Status	Ready	4 00000000h	8.0	0000h	DF01001Ch	00	
17.297.822.640.500	[Down 1, Up 1]	NVMe: Set Features	Successful Completion	0	8.0	0000h	8CD2B000h	03	
17.297.822.648.500	[Down 1, Up 1]	NVMe: Read Controller Status	Ready	4 00000000h	8.0	0000h	DF01001Ch	00	
17.298.831.087.500	[Down 1, Up 1]	NVMe: Identify	Successful Completion	4,096 ba4d4ab0h 444d5643h 3...	8.0	0000h	8CD2B040h	03	
17.298.831.140.000	[Down 1, Up 1]	NVMe: Read Controller Status	Ready	4 00000000h	8.0	0000h	DF01001Ch	00	
17.299.837.980.000	[Down 1, Up 1]	NVMe: Identify	Successful Completion	4,096 ba4d4ab0h 00000000h b...	8.0	0000h	8CD2B080h	03	
17.299.838.020.500	[Down 1, Up 1]	NVMe: Read Controller Status	Ready	4 00000000h	8.0	0000h	DF01001Ch	00	
17.300.842.759.500	[Down 1, Up 1]	NVMe: Create I/O Completion Queue	Successful Completion	0	8.0	0000h	8CD2B0C0h	03	
17.300.842.810.500	[Down 1, Up 1]	NVMe: Read Controller Status	Ready	4 00000000h	8.0	0000h	DF01001Ch	00	
17.301.847.501.500	[Down 1, Up 1]	NVMe: Create I/O Submission Queue	Successful Completion	0	8.0	0000h	8CD2B100h	03	
17.301.847.544.000	[Down 1, Up 1]	NVMe: Read Controller Status	Ready	4 00000000h	8.0	0000h	DF01001Ch	00	
17.302.863.308.500	[Down 1, Up 1]	NVMe: Read	Successful Completion	512 23232323h 23232323h 2...	8.0	0000h	8CD1E000h	03	
17.302.863.308.500	Down 1	Submission Queue Doorbell Ring; TLP Memory Write Request (0xcfb);							
17.302.863.496.000	Up 1	Command Fetch; TLP Memory Read Request (0xd37);							
17.302.863.923.500	Down 1	Read; TLP Completion With Data (0xcfa);							
17.302.936.311.500	Up 1	Data; TLP Memory Write Request (0xd39); 128 bytes							
17.302.936.354.500	Up 1	Data; TLP Memory Write Request (0xd3a); 128 bytes							
17.302.936.397.000	Up 1	Data; TLP Memory Write Request (0xd3b); 128 bytes							
17.302.936.438.000	Up 1	Data; TLP Memory Write Request (0xd3c); 128 bytes							
17.302.936.579.000	Up 1	Command Completion; TLP Memory Write Request (0xd3d);							
17.303.865.287.000	Down 1	Completion Queue Doorbell Ring; TLP Memory Write Request (0xcfb);							
17.307.863.358.000	[Down 1, Up 1]	NVMe: Read Controller Status	Ready	4 00000000h	8.0	0000h	DF01001Ch	00	

